WHAT IS CLAIMED IS:

1. A zeroing circuit for a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the zeroing circuit comprising:

logic for zeroing out a specified number of most significant bits ("MSBs") of a selected portion of the debug data based on a mask generated by a mask generator block; and

means for providing a selection control signal to the mask generator block, the selection control signal operating to select the specified number of MSBs for zeroing.

2. The zeroing circuit of claim 1 wherein the logic for zeroing out a specified number of MSBs comprises logic for ANDing the inverted value of each bit of the mask with a corresponding bit of the selected portion of the debug data.

3. The zeroing circuit of claim 2 wherein the selection control signal is three bits in length.

4. The zeroing circuit of claim 2 wherein the mask generator block is implemented using a plurality of multiplexers, the selection control signal operating to select inputs of each of the multiplexers.

5. The zeroing circuit of claim 2 wherein the logic for ANDing comprises an AND circuit.

6. The zeroing circuit of claim 5 wherein the AND circuit comprises a plurality of 2-input AND gates.

7. The zeroing circuit of claim 6 wherein each of the 2-input AND gates comprises an inverter input connected to receive a bit of the mask and an input connected to receive a corresponding bit of the selected portion of the debug data.

8. The zeroing circuit of claim 1 wherein the mask and the selected portion of the debug data are each *S*-bits in length.

9. The zeroing circuit of claim 1 wherein *S* is equal to eight.

10. A zeroing circuit for a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the zeroing circuit comprising:

means for providing a signal specifying a number of most significant bits ("MSBs") of a selected portion of the debug data to be zeroed out; and

means for zeroing out the specified number of MSBs of the selected portion of the debug data based on the signal.

11. The zeroing circuit of claim 10 further comprising:

means for creating a mask, wherein a value of a control signal input to the means for creating a mask specifies a number of the MSBs of the mask that are to be set to one; and

means for ANDing the inverted value of each bit of the mask with a corresponding bit of the selected portion of the debug data.

12. The zeroing circuit of claim 11 wherein the control signal is three bits in length.

13. The zeroing circuit of claim 11 wherein the means for creating a mask is implemented using a plurality of multiplexers, wherein the control signal is input to select inputs of each of the multiplexers.

14. The zeroing circuit of claim 11 wherein the means for ANDing comprises an AND circuit.

15. The zeroing circuit of claim 14 wherein the AND circuit comprises a plurality of 2-input AND gates.

16. The zeroing circuit of claim 15 wherein each of the 2-input AND gates comprises an inverter input connected to receive a bit of the mask and an input connected to receive a corresponding bit of the selected portion of the debug data.

17. The zeroing circuit of claim 10 wherein the mask and the selected portion of the debug data are each *S*-bits in length.

18. The zeroing circuit of claim 10 wherein *S* is equal to eight.

19. A method of implementing a zeroing circuit for a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the method comprising:

generating a control signal indicative of a number of most significant bits ("MSBs") of a selected portion of the debug data to be set to zero;

creating an *S*-bit mask based on the control signal; and

generating an *S*-bit zeroed data signal using the *S*-bit mask, wherein the S-bit zeroed data signal comprises the selected portion of the debug data with the indicated number of MSBs thereof set to zero.

20. The method of claim 19 wherein a number of the MSBs of the mask that are set to one is equal to the value of the control signal, with the remaining least significant bits ("LSBs") thereof set to zero.

21. The method of claim 19 wherein the operation of generating an *S*-bit zeroed data signal comprises ANDing each bit of the inverse of the mask with a bit of the selected debug data portion, the result of each AND operation giving rise to a corresponding bit of the zeroed data signal.

22. The method of claim 19 wherein *S* is equal to eight.

23. The method of claim 2 wherein the control signal is three bits in length.